

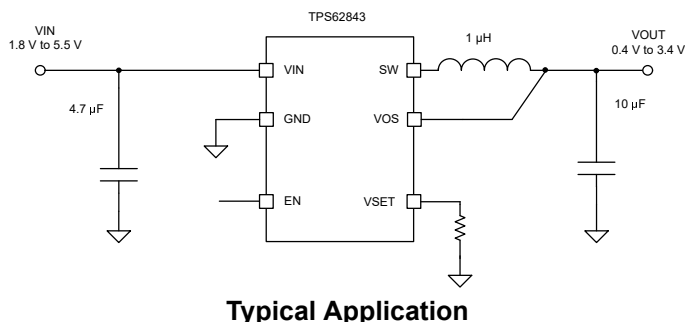
# TPS62843 1.8-V to 5.5-V, 600-mA, 275-nA I<sub>Q</sub>, Small-Size Step-Down Converters

## 1 Features

- 1.8-V to 5.5-V input voltage range
- 0.4-V to 3.6-V output voltage range
- 275-nA typical quiescent current
- 600-mA output current
- 1% output voltage accuracy
- 4-nA typical shutdown current
- Output discharge
- VSET pin-selectable output voltage through a single resistor
  - TPS628436: 0.4 V to 0.8 V
  - TPS628437: 0.8 V to 1.8 V
  - TPS628438: 1.8 V to 3.6 V
- Optimized for small passive components
  - 1- $\mu$ H inductor
  - Down to 4.7- $\mu$ F C<sub>OUT</sub>
- High PSRR (up to 83 dB)
- Low output voltage ripple in power save mode
- RF-friendly and fast transient DCS-Control
- Automatic transition to no ripple 100% mode
- 0603-inductor and 0402-capacitor size supported
- Tiny 6-pin, 0.35-mm pitch WCSP package with 0.84mm<sup>2</sup> size
- Pin-to-pin compatible to the [TPS6280x](#) family (1 A) in WCSP package
- Available in a 1.60-mm × 1.60-mm SOT563 package

## 2 Applications

- [Wearable electronics](#)
- [Headsets, headphones, and earbuds](#)
- [Mobile phones](#)
- [Medical sensor patches](#)
- [Hearing aid](#)



## 3 Description

The TPS62843 is a high-efficiency, step-down converter family with ultra-low operating quiescent current of typically 275 nA. The device features a 4-nA shutdown (typical) current when disabled.

The device uses DCS-Control with a low and RF-friendly output voltage ripple to power radios.

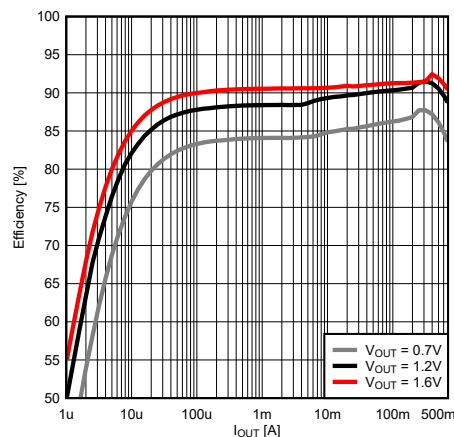
The device operates with a typical switching frequency of 1.5 MHz and extends a high efficiency at light-load down to 100- $\mu$ A load current and below.

3 x 18 pre-defined output voltages can be selected by connecting a resistor to the VSET pin, making the family usable across various applications with a minimum set of passive components.

### Device Information

| PART NUMBER <sup>(3)</sup> | V <sub>OUT</sub> RANGE | PACKAGE <sup>(1)</sup>            | BODY SIZE (NOM)                   |
|----------------------------|------------------------|-----------------------------------|-----------------------------------|
| TPS628436                  | 0.4 V – 0.8 V          | YKA<br>(DSBGA, 6)                 | 0.80 mm ×<br>1.05 mm ×<br>0.40 mm |
| TPS628437                  | 0.8 V – 1.8 V          |                                   |                                   |
| TPS628438                  | 1.8 V – 3.6 V          |                                   |                                   |
| TPS628436                  | 0.4 V – 0.8 V          | DRL<br>(SOT563, 6) <sup>(2)</sup> | 1.6 mm × 1.6<br>mm × 0.6 mm       |
| TPS628437                  | 0.8 V – 1.8 V          |                                   |                                   |
| TPS628438                  | 1.8 V – 3.6 V          |                                   |                                   |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) Advance Information (not Production Data).
- (3) See the [Device Comparison Table](#).



**Efficiency vs Output Current at 3.6 V<sub>IN</sub>**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision A (May 2023) to Revision B (September 2023)</b> | <b>Page</b> |
|--|-------------|
| • Added SOT563 package to the document.....                              | 1           |

| <b>Changes from Revision * (January 2022) to Revision A (May 2023)</b>     | <b>Page</b> |
|--|-------------|
| • Changed document status from Advance Information to Production Data..... | 1           |

## 5 Device Comparison Table

| Device    | Fixed $V_{OUT}$<br>$V_{SET} = GND$ | Selectable Output Voltages    | $f_{sw}$<br>[MHz] | Soft Start $t_{SS}$ | Inductor  |
|-----------|------------------------------------|-------------------------------|-------------------|---------------------|-----------|
| TPS628436 | 1.0 V                              | 0.4 V – 0.8 V in 25-mV steps  | 1.5               | 400 $\mu$ s         | 1 $\mu$ H |
| TPS628437 | 1.8 V                              | 0.8 V – 1.6 V in 50-mV steps  | 1.5               | 800 $\mu$ s         | 1 $\mu$ H |
| TPS628438 | 3.6 V                              | 1.8 V – 3.4 V in 100-mV steps | 1.5               | 800 $\mu$ s         | 1 $\mu$ H |

## 6 Pin Configuration and Functions

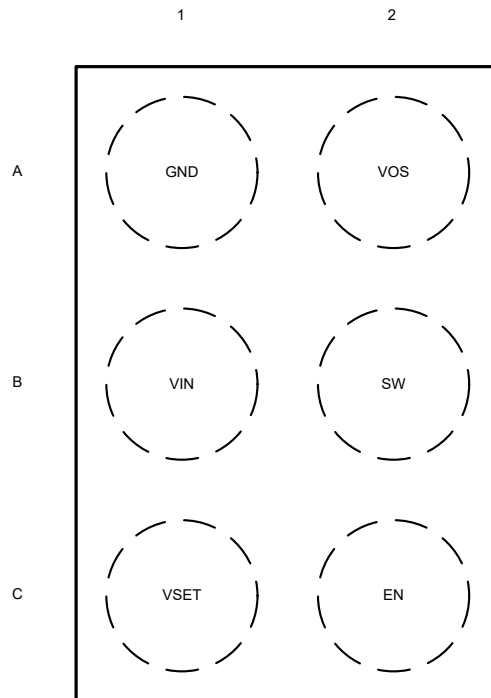


Figure 6-1. 6-Pin DSBGA YKA Package (Top View)

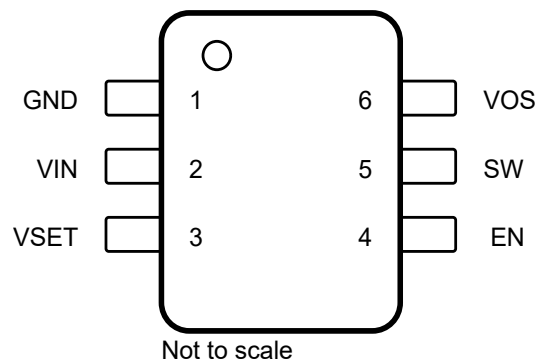


Figure 6-2. 6-Pin DRL SOT563 Package (Top View)

Table 6-1. Pin Functions

| PIN  |     | TYPE | DESCRIPTION   |
|------|-----|------|---|
| NAME | NO. |      |   |
| GND  | A1  | PWR  | GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.   |
| VIN  | B1  | PWR  | V <sub>IN</sub> power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor is required.  |
| VSET | C1  | I    | Connecting a resistor to GND selects a pre-defined output voltage.  |
| VOS  | A2  | I    | Output voltage sense pin for the internal feedback divider network and regulation loop. This pin also discharges V <sub>OUT</sub> by an internal MOSFET when the converter is disabled. Connect this pin directly to the output capacitor with a short trace. |
| SW   | B2  | O    | The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.   |
| EN   | C2  | I    | A high level enables the devices and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled once the device has started up.  |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) <sup>(1)</sup>

|                  |  | MIN  | MAX                     | UNIT |
|------------------|--|------|-------------------------|------|
| Pin voltage      | V <sub>IN</sub>                        | -0.3 | 6                       | V    |
| Pin voltage      | SW, DC                                 | -0.3 | V <sub>IN</sub> + 0.3 V | V    |
| Pin voltage      | SW, transient < 10 ns, while switching | -2.5 | 9                       | V    |
| Pin voltage      | EN, VSET                               | -0.3 | 6                       | V    |
| Pin voltage      | VOS                                    | -0.3 | 5                       | V    |
| T <sub>J</sub>   | Operating junction temperature         | -40  | 150                     | °C   |
| T <sub>stg</sub> | Storage temperature                    | -55  | 150                     | °C   |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 7.2 ESD Ratings

|                    |                         |   | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>     | ±2000 | V    |
|                    |                         | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

|                   |   | MIN  | NOM | MAX  | UNIT   |
|-------------------|---|------|-----|------|--------|
| V <sub>IN</sub>   | Supply voltage V <sub>IN</sub>  | 1.8  |     | 5.5  | V      |
| I <sub>OUT</sub>  | Output current  |      |     | 0.6  | A      |
| L                 | Effective inductance  | 0.7  | 1.0 | 1.2  | μH     |
| C <sub>OUT</sub>  | Effective output capacitance  | 4    |     | 25   | μF     |
| C <sub>IN</sub>   | Effective input capacitance   | 0.5  | 4.7 |      | μF     |
| C <sub>VSET</sub> | External parasitic capacitance at VSET pin                                  |      |     | 30   | pF     |
| R <sub>SET</sub>  | Resistance range for external resistor at VSET pin (E96 1% resistor values) | 10   |     | 249  | kΩ     |
|                   | External resistor tolerance E96 series at VSET pin                          |      |     | 1%   |        |
|                   | E96 resistor series temperature coefficient (TCR)                           | -200 |     | +200 | ppm/°C |
| T <sub>J</sub>    | Operating junction temperature range  | -40  |     | 125  | °C     |

## 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | YKA (DSBGA) 6 PINS | DRL (SOT563) 6 PINS | UNIT |
|-------------------------------|--|--------------------|---------------------|------|
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 147.7              | 138.3               | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 1.7                | 57.3                | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 47.5               | 24.7                | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.5                | 1.4                 | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 47.6               | 24.4                | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | –                  | –                   | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

T<sub>J</sub> = –40°C to +125°C, V<sub>IN</sub> = 1.8 V to 5.5 V. Typical values are at T<sub>J</sub> = 25°C, V<sub>IN</sub> = 3.6 V and V<sub>OUT</sub> = 0.7 V (unless otherwise noted)

| PARAMETER             |   | TEST CONDITIONS  | MIN  | TYP  | MAX  | UNIT |
|-----------------------|---|--|------|------|------|------|
| <b>SUPPLY</b>         |   |  |      |      |      |      |
| I <sub>Q</sub>        | Operating Quiescent Current (Power Save Mode) | Non-switching, V <sub>EN</sub> = V <sub>IN</sub> , I <sub>OUT</sub> = 0 μA, T <sub>J</sub> = –40°C to 85°C |      | 275  | 1500 | nA   |
|                       |   | Switching, V <sub>EN</sub> = V <sub>IN</sub> , I <sub>OUT</sub> = 0 μA, V <sub>OUT</sub> = 0.7 V           |      | 350  |      | nA   |
| I <sub>SD</sub>       | Shutdown Current                              | V <sub>EN</sub> = 0 V, VSET = GND, T <sub>J</sub> = –40°C to 85°C  |      | 4    | 850  | nA   |
| <b>UVLO</b>           |   |  |      |      |      |      |
| V <sub>UVLO(R)</sub>  | Undervoltage Lockout Rising Threshold         | V <sub>IN</sub> rising, I <sub>OUT</sub> = 0 μA  |      | 1.75 | 1.8  | V    |
| V <sub>UVLO(F)</sub>  | Undervoltage Lockout Falling Threshold        | V <sub>IN</sub> falling, I <sub>OUT</sub> = 0 μA   |      | 1.65 | 1.7  | V    |
| V <sub>UVLO(H)</sub>  | Undervoltage Lockout Hysteresis               |  |      | 100  |      | mV   |
| <b>VSET PIN</b>       |   |  |      |      |      |      |
| V <sub>SET(LKG)</sub> | VSET Input leakage current                    | T <sub>J</sub> = –40°C to 85°C   |      | 10   | 800  | nA   |
| V <sub>SET(H)</sub>   | VSET High-level detection                     | Voltage at VSET during startup   | 1.0  |      |      | V    |
| R <sub>SET</sub>      | RSET accuracy                                 | T <sub>J</sub> = –20°C to 125°C  | –4   |      | 4    | %    |
| R <sub>SET</sub>      | RSET accuracy                                 | T <sub>J</sub> = –40°C to 125°C  | –3.5 |      | 3.5  | %    |
| <b>ENABLE</b>         |   |  |      |      |      |      |
| V <sub>EN(R)</sub>    | EN voltage rising threshold                   | EN rising, enable switching  | 0.8  |      |      | V    |
| V <sub>EN(F)</sub>    | EN voltage falling threshold                  | EN falling, disable switching  |      |      | 0.4  | V    |
| V <sub>EN(LKG)</sub>  | EN Input leakage current                      | V <sub>EN</sub> > 0.8 V, T <sub>J</sub> = –40°C to 85°C  |      | 1    | 25   | nA   |
| R <sub>EN;PD</sub>    | EN internal pull-down resistance              | EN pin to GND  | 425  | 500  |      | kΩ   |
| <b>VOUT VOLTAGE</b>   |   |  |      |      |      |      |
| V <sub>OUT</sub>      | DC Output voltage accuracy                    | PWM operation, T <sub>J</sub> = –20°C to 125°C   | –1   |      | +1   | %    |
| V <sub>OUT</sub>      | DC Output voltage accuracy                    | PWM operation, T <sub>J</sub> = –40°C to 125°C   | –1.5 |      | +1.5 | %    |
| V <sub>OUT</sub>      | TPS628436                                     |  | 0.4  |      | 0.8  | V    |
|                       | TPS628437                                     |  | 0.8  |      | 1.8  | V    |
|                       | TPS628438                                     |  | 1.8  |      | 3.6  | V    |
| I <sub>VOS(LKG)</sub> | VOS input leakage current                     | TPS628436, V <sub>EN</sub> = V <sub>IN</sub> , V <sub>VOS</sub> = 0.7 V, T <sub>J</sub> = –40°C to 85°C    |      |      | 100  | nA   |
|                       |   | TPS628437, V <sub>EN</sub> = V <sub>IN</sub> , V <sub>VOS</sub> = 1.2 V, T <sub>J</sub> = –40°C to 85°C    |      | 100  | 250  | nA   |
|                       |   | TPS628438, V <sub>EN</sub> = V <sub>IN</sub> , V <sub>VOS</sub> = 3.3 V, T <sub>J</sub> = –40°C to 85°C    |      | 275  | 450  | nA   |
| f <sub>SW</sub>       |   | I <sub>OUT</sub> = 400mA   |      | 1.5  |      | MHz  |
| <b>STARTUP</b>        |   |  |      |      |      |      |
| t <sub>SS</sub>       | TPS628436 soft-start time                     | From V <sub>OUT</sub> = 0% to V <sub>OUT</sub> = 95% of V <sub>OUT</sub> nominal                           |      | 0.45 | 0.6  | ms   |
|                       | TPS628438 soft-start time                     |  |      | 1.0  | 1.4  |      |
|                       | TPS628437 soft-start time                     |  |      | 0.7  | 1.0  |      |

## 7.5 Electrical Characteristics (continued)

$T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $V_{IN} = 1.8\text{ V}$  to  $5.5\text{ V}$ . Typical values are at  $T_J = 25^{\circ}\text{C}$ ,  $V_{IN} = 3.6\text{ V}$  and  $V_{OUT} = 0.7\text{ V}$  (unless otherwise noted)

| PARAMETER                     |                                      | TEST CONDITIONS  | MIN  | TYP | MAX  | UNIT               |
|-------------------------------|--------------------------------------|--|------|-----|------|--------------------|
| $t_{\text{Startup\_delay}}$   | EN HIGH to start of switching delay  | R2D = GND  |      | 330 | 560  | $\mu\text{s}$      |
| <b>POWER STAGE</b>            |                                      |  |      |     |      |                    |
| $R_{\text{DSON(HS)}}$         | High-side MOSFET on-resistance       | $V_{IN} = 3.6\text{V}$ , $I_{\text{OUT}} = 300\text{ mA}$  |      | 170 | 260  | $\text{m}\Omega$   |
| $R_{\text{DSON(LS)}}$         | Low-side MOSFET on-resistance        | $V_{IN} = 3.6\text{V}$ , $I_{\text{OUT}} = 300\text{ mA}$  |      | 70  | 115  | $\text{m}\Omega$   |
| ILKG_SW                       | Leakage Current into SW-Pin          | $V_{\text{SW}} = 0.7\text{V}$ , $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$                                    |      | 0   | 35   | nA                 |
| ILKG_SW                       | Leakage Current into SW-Pin          | $V_{\text{SW}} = 1.2\text{V}$ , $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$                                    |      | 0   | 45   | nA                 |
| ILKG_SW                       | Leakage Current into SW-Pin          | $V_{\text{VIN}} > V_{\text{SW}}$ , $V_{\text{SW}} = 3.3\text{V}$ , $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ |      | 0   | 45   | nA                 |
| <b>OVERCURRENT PROTECTION</b> |                                      |  |      |     |      |                    |
| $I_{\text{HS(OC)}}$           | High-side peak current limit         | $V_{IN} \geq 2.2\text{V}$  | 0.9  | 1.1 | 1.3  | A                  |
| $I_{\text{LS(OC)}}$           | Low-side valley current limit        | $V_{IN} \geq 2.2\text{V}$  | 0.79 | 1.0 | 1.11 | A                  |
| <b>OUTPUT DISCHARGE</b>       |                                      |  |      |     |      |                    |
| $R_{\text{DSCH\_VOS}}$        | Output discharge resistor on VOS pin | $V_{\text{EN}} = \text{GND}$ , $I(\text{VOS}) = -10\text{mA}$  |      | 7   | 22   | $\Omega$           |
| <b>THERMAL SHUTDOWN</b>       |                                      |  |      |     |      |                    |
| $T_{\text{J(SD)}}$            | Thermal shutdown threshold           | Temperature rising   |      | 160 |      | $^{\circ}\text{C}$ |
| $T_{\text{J(HYS)}}$           | Thermal shutdown hysteresis          |  |      | 20  |      | $^{\circ}\text{C}$ |

## 7.6 Typical Characteristics

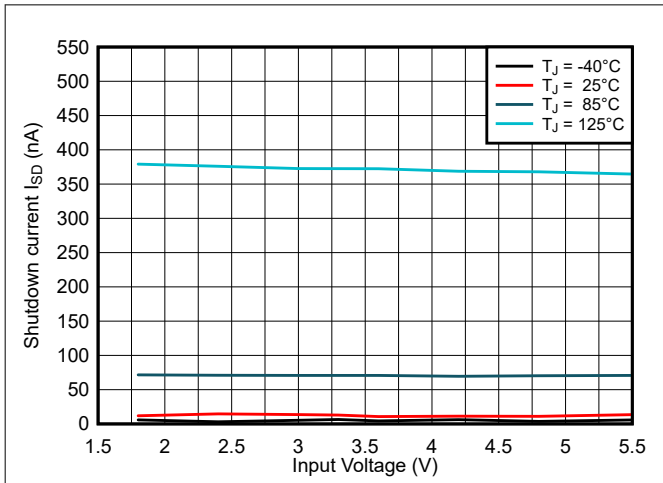


Figure 7-1. Shutdown Current  $I_{SD}$

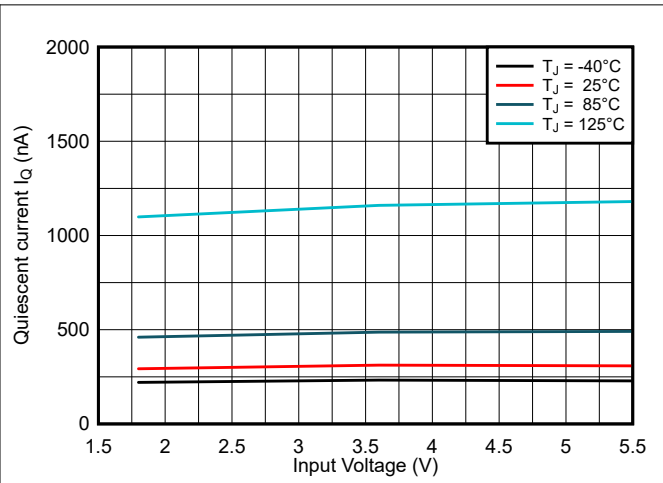


Figure 7-2. Quiescent Current  $I_Q$

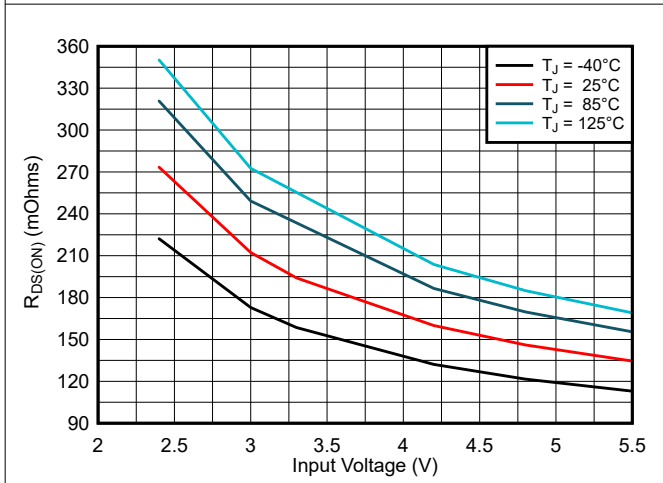


Figure 7-3. High Side Switch Drain Source Resistance  $R_{DS(ON)}$

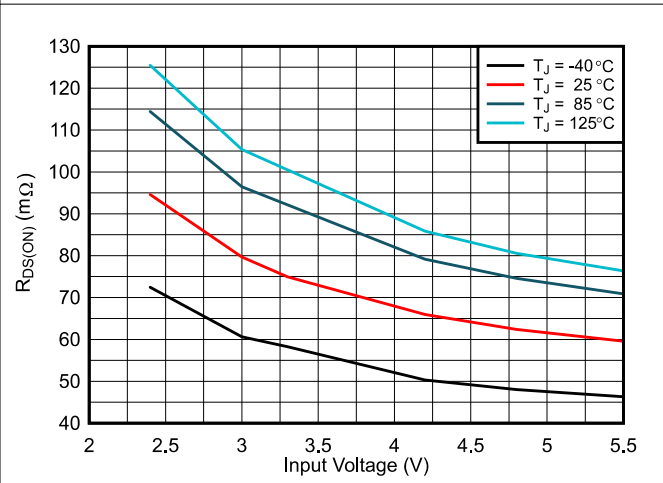


Figure 7-4. Low Side Switch Drain Source Resistance  $R_{DS(ON)}$

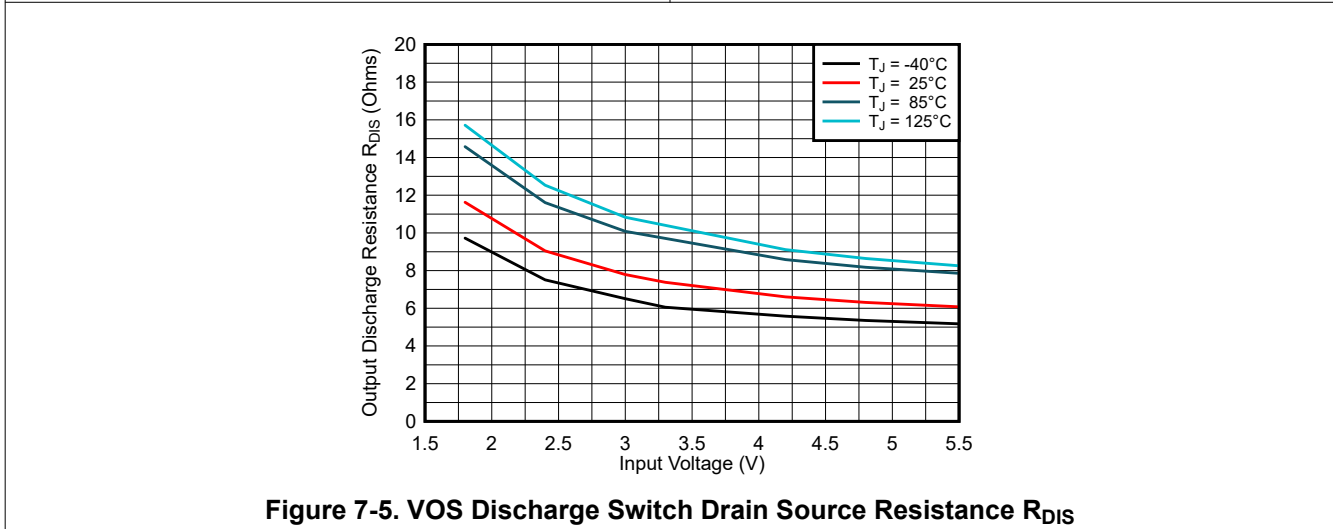


Figure 7-5. VOS Discharge Switch Drain Source Resistance  $R_{DIS}$



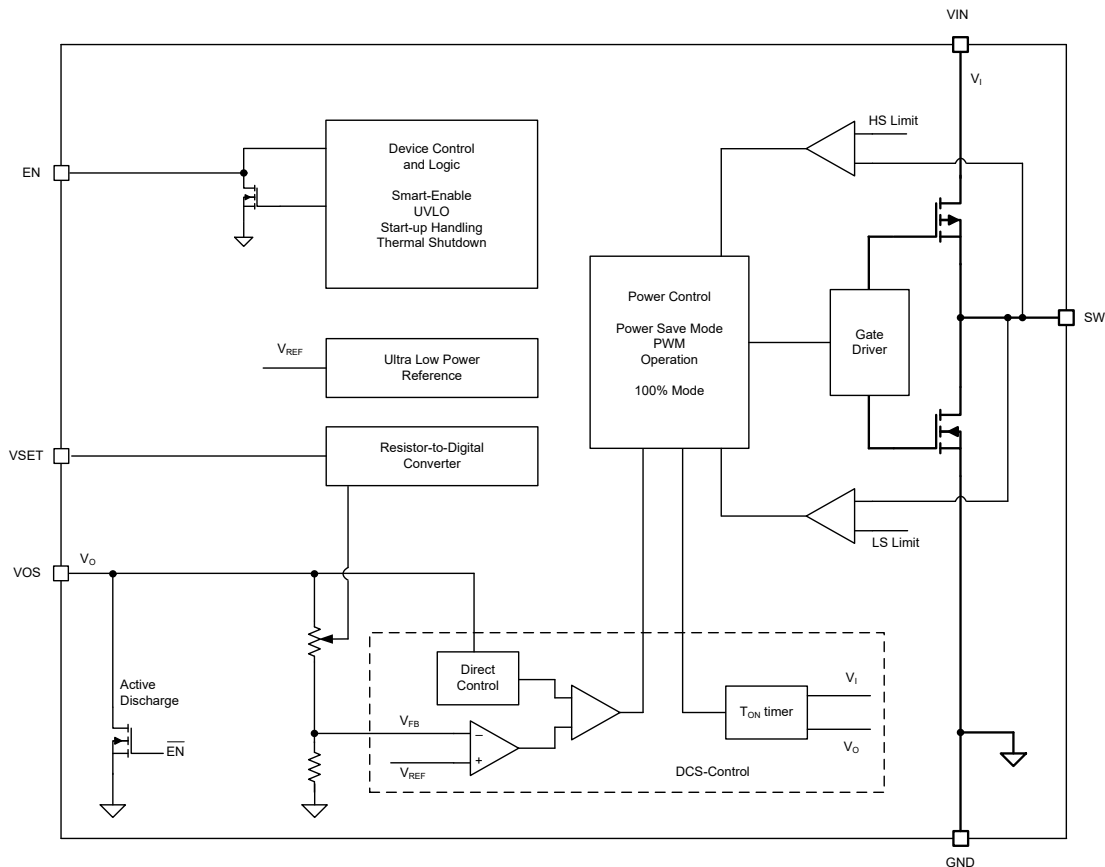
## 8 Detailed Description

### 8.1 Overview

The TPS62843 is a high-frequency, synchronous step-down converter with ultra-low quiescent current of typically 275 nA in a 0.84-mm<sup>2</sup> chip size. The device operates with a tiny 1-μH inductor and 10-μF output capacitor over the entire recommended operation range to provide one of the industry's smallest chip and solution size.

Using TI's DCS-Control topology, the device extends the high efficiency operation area down to microamperes of load current during power save mode operation. TI's DCS-Control (Direct Control with Seamless Transition into power save mode) is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control are excellent AC load regulation and transient response, low output ripple voltage, and a seamless transition between PFM and PWM mode operation. DCS-Control includes an AC loop that senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

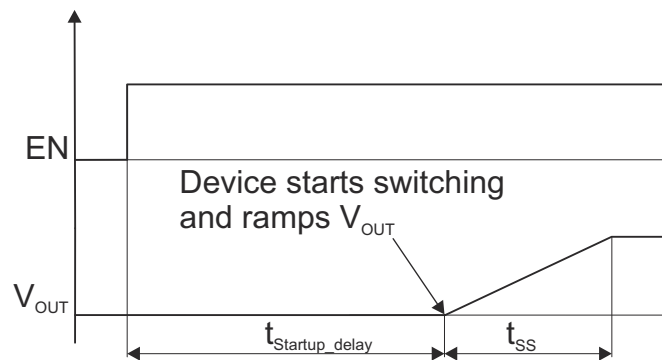
### 8.3.1 Smart Enable and Shutdown (EN)

An internal 500-k $\Omega$  resistor pulls the EN pin to GND and avoids floating the pin. This action prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin once the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again.

### 8.3.2 Soft Start

After the device has been enabled with EN high, the device initializes and powers up its internal circuits. This action occurs during the regulator start-up delay time,  $t_{\text{Startup\_delay}}$ . After  $t_{\text{Startup\_delay}}$  expires, the internal soft-start circuitry ramps up the output voltage within the soft-start time,  $t_{\text{SS}}$ . See [Figure 8-1](#).

The start-up delay time,  $t_{\text{Startup\_delay}}$ , varies depending on the selected VSET value. The start-up delay is shortest with VSET = 0 and longest with VSET = 16.



**Figure 8-1. Device Start-Up**

### 8.3.3 VSET Pin: Output Voltage Selection

The output voltage is set with a single external resistor connected between the VSET pin and GND. After the device has been enabled and the control logic as well as the internal reference have been powered up, a R2D (resistor-to-digital) conversion is started to detect the external resistor,  $R_{\text{SET}}$ , within the regulator start-up delay time,  $t_{\text{Startup\_delay}}$ . An internal current source applies current through the external resistor and an internal ADC reads back the resulting voltage level. Depending on the level, an internal feedback divider network is selected to set the correct output voltage. After this R2D conversion is finished, the current source is turned off to avoid current flow through the external resistor. The circuit can detect resistive values, high-level, low-level, and a pin-open.

For a proper reading, ensure that there is no additional current path or capacitance greater than 30 pF total to GND during R2D conversion. Otherwise, the additional current to GND is interpreted as a lower resistor value and a false output voltage is set. [Table 8-1](#) lists the correct resistor values for  $R_{\text{SET}}$  to set the appropriate output voltages. The R2D converter is designed to operate with resistor values out of the E96 table and requires 1% resistor value accuracy. The external resistor  $R_{\text{SET}}$  is not a part of the regulator feedback loop and has therefore no impact on the output voltage accuracy. Ensure that there is no other leakage path than the  $R_{\text{SET}}$  resistor at the VSET pin during an undervoltage lockout event. Otherwise, a false output voltage is set.

**Table 8-1. Output Voltage Setting**

| VSET | Output Voltage Setting [V] |           |           | R <sub>SET</sub> [Ω] |
|------|----------------------------|-----------|-----------|----------------------|
|      | TPS628436                  | TPS628437 | TPS628438 |                      |
| 1    | 0.400                      | 0.80      | 1.8       | 10.0 k               |
| 2    | 0.425                      | 0.85      | 1.9       | 12.1 k               |
| 3    | 0.450                      | 0.90      | 2.0       | 15.4 k               |
| 4    | 0.475                      | 0.95      | 2.1       | 18.7 k               |
| 5    | 0.500                      | 1.00      | 2.2       | 23.7 k               |
| 6    | 0.525                      | 1.05      | 2.3       | 28.7 k               |
| 7    | 0.550                      | 1.10      | 2.4       | 36.5 k               |
| 8    | 0.575                      | 1.15      | 2.5       | 44.2 k               |
| 9    | 0.600                      | 1.20      | 2.6       | 56.2 k               |
| 10   | 0.625                      | 1.25      | 2.7       | 68.1 k               |
| 11   | 0.650                      | 1.30      | 2.8       | 86.6 k               |
| 12   | 0.675                      | 1.35      | 2.9       | 105.0 k              |
| 13   | 0.700                      | 1.40      | 3.0       | 133.0 k              |
| 14   | 0.725                      | 1.45      | 3.1       | 162.0 k              |
| 15   | 0.750                      | 1.50      | 3.2       | 205.0 k              |
| 16   | 0.775                      | 1.55      | 3.3       | 249.0 k or larger    |
| 17   | 0.8                        | 1.6       | 3.4       | V <sub>IN</sub>      |
| 0    | 1.0                        | 1.8       | 3.6       | GND                  |

### 8.3.4 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input voltage of 1.7 V (maximum) with falling V<sub>IN</sub>. The device starts at an input voltage of 1.8 V (maximum) rising V<sub>IN</sub>. After the device re-enters operation out of an undervoltage lockout condition, the device behaves like it does being enabled. The internal control logic is powered up and the external resistor at the VSET pin is read out.

### 8.3.5 Switch Current Limit, Short-Circuit Protection

The TPS62843 integrates a current limit on the high-side and low-side MOSFETs to protect the device against overload or short circuit conditions. The current in the switches is monitored cycle by cycle. If the high-side MOSFET current limit, I<sub>LIMF</sub> trips, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. After the inductor current through the low-side switch decreases beneath the low-side MOSFET current limit, I<sub>LIMF</sub>, the low-side MOSFET is turned off and the high-side MOSFET turns on again.

### 8.3.6 Thermal Shutdown

The junction temperature (T<sub>J</sub>) of the device is monitored by an internal temperature sensor. If T<sub>J</sub> exceeds the thermal shutdown temperature, T<sub>SD</sub>, of 160°C (typical), the device enters thermal shutdown. Both the high-side and low-side power FETs are turned off. When T<sub>J</sub> decreases below the hysteresis amount of typically 20°C, the converter resumes operation, beginning with a soft start to the originally set V<sub>OUT</sub> (there is no R2D conversion of R<sub>SET</sub>). The thermal shutdown is not active in power save mode.

### 8.3.7 Output Voltage Discharge

The purpose of the output discharge function is to ensure a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0 V.

The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled. The minimum supply voltage required to keep the discharge function active is V<sub>IN</sub> > V<sub>TH\_UVLO</sub>.

## 8.4 Device Functional Modes

### 8.4.1 Power Save Mode Operation

The DCS-Control topology supports power save mode operation. At light loads, the device operates in PFM (pulse frequency modulation) mode that generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shut down to achieve the lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption is reduced to typically 275 nA. This low quiescent current consumption is achieved by an ultra-low power voltage reference, an integrated high impedance feedback divider network, and an optimized power save mode operation.

In PFM mode, the switching frequency varies linearly with the load current. At medium and high load conditions, the device enters automatically PWM (pulse width modulation) mode and operates in continuous conduction mode with a nominal switch frequency  $f_{sw}$  of typically 1.5 MHz. The switching frequency in PWM mode is controlled and depends on  $V_{IN}$  and  $V_{OUT}$ . The boundary between PWM and PFM mode is when the inductor current becomes discontinuous.

If the load current decreases, the converter seamlessly enters PFM mode to maintain high efficiency down to very light loads. Because DCS-Control supports both operation modes within one single building block, the transition from PWM to PFM mode is seamless with minimum output voltage ripple.

### 8.4.2 100% Mode Operation

The duty cycle of the buck converter operating in PWM mode is given as  $D = V_{OUT}/V_{IN}$ . The duty cycle increases as the input voltage comes close to the output voltage. In 100% duty cycle mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences.

## 9 Application and Implementation

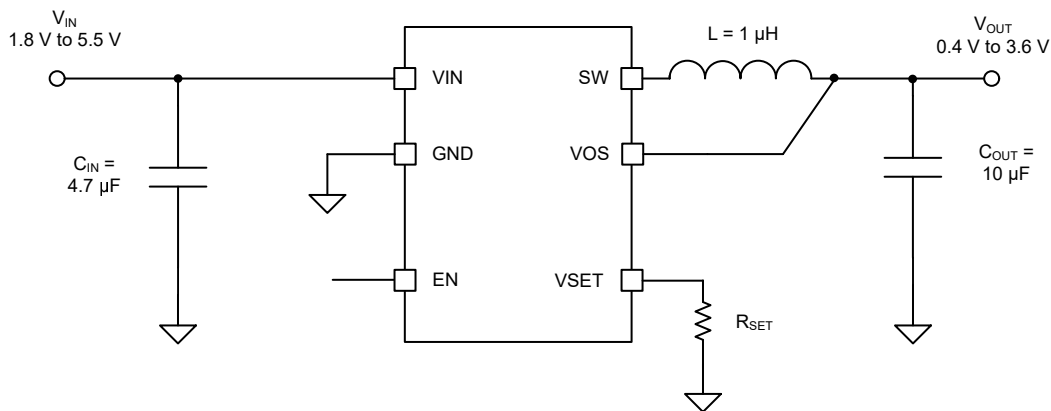
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The following sections discuss the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

### 9.2 Typical Application



**Figure 9-1. TPS62843 Typical Application Circuit**

#### 9.2.1 Design Requirements

Table 9-1 shows the list of components for the application circuit and the characteristic application curves.

**Table 9-1. Components for Application Characteristic Curves**

| Reference                             | Description                             | Value  | Size Code Inch [metric L × W × T] | Manufacturer |
|---------------------------------------|---|--------|-----------------------------------|--------------|
| TPS628436,<br>TPS628437,<br>TPS628438 | 275 nA-I <sub>Q</sub> buck converter    |        | [1.05 mm × 0.8 mm × 0.4 mm]       | TI           |
| C <sub>IN</sub>                       | Ceramic capacitor<br>GRM155R60J475ME47D | 4.7 μF | 0402 [1.0 mm × 0.5 mm × 0.5 mm]   | Murata       |
| L                                     | Inductor DFE201610-1R0M                 | 1 μH   | 0806 [2.0 mm × 1.6 mm × 1.0 mm]   | Murata       |
| C <sub>OUT</sub>                      | Ceramic capacitor<br>GRM155R60J106ME15D | 10 μF  | 0402 [1.0 mm × 0.5 mm × 0.5 mm]   | Murata       |
| R <sub>SET</sub>                      | See voltage setting table               |        | 0402 [1.0 mm × 0.5 mm × 0.5 mm]   |              |

#### 9.2.2 Detailed Design Procedure

Follow the passive component selection per the typical application circuit.

### 9.2.3 Application Curves

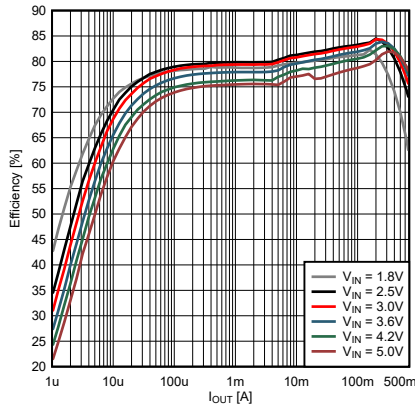


Figure 9-2. Efficiency at 0.4 V<sub>OUT</sub>

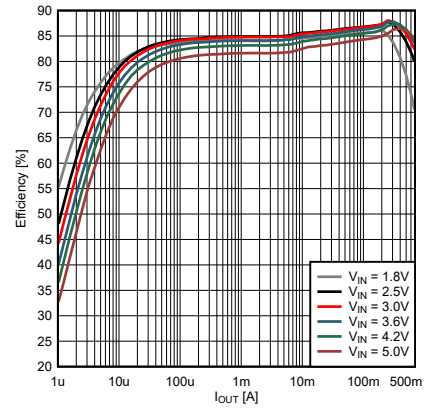


Figure 9-3. Efficiency at 0.7 V<sub>OUT</sub>

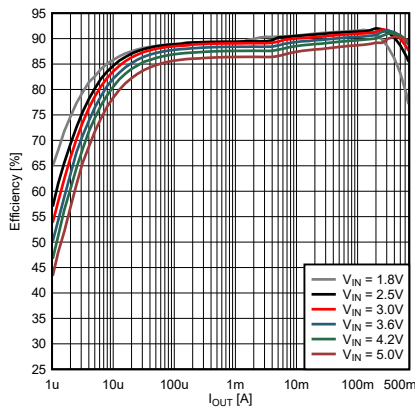


Figure 9-4. Efficiency at 1.2 V<sub>OUT</sub>

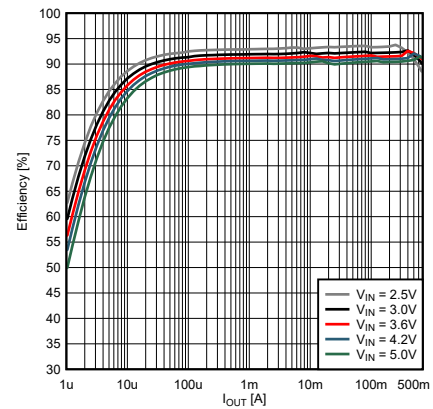


Figure 9-5. Efficiency at 1.8 V<sub>OUT</sub>

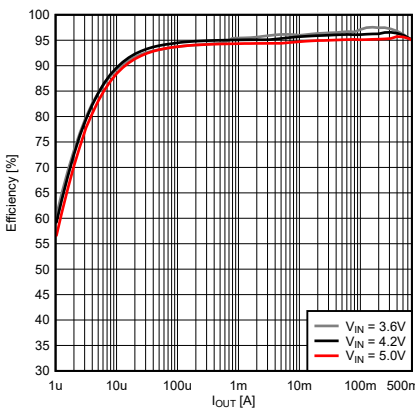


Figure 9-6. Efficiency at 3.3 V<sub>OUT</sub>

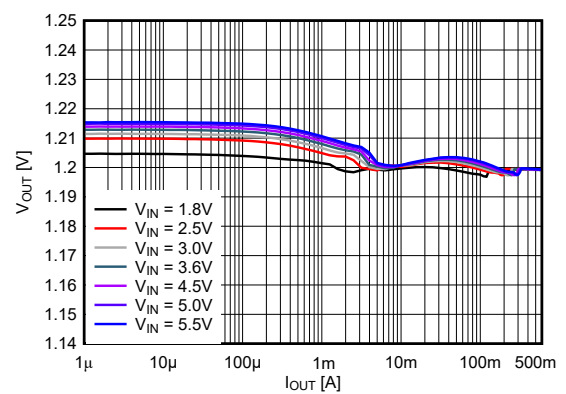
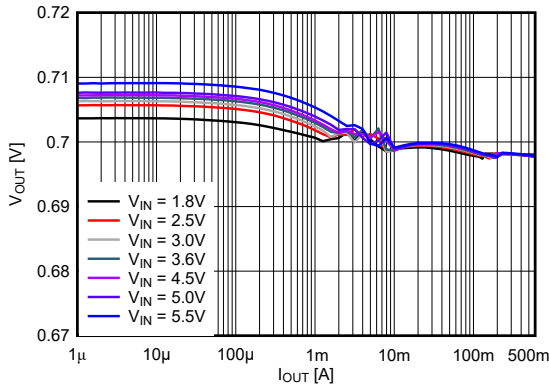
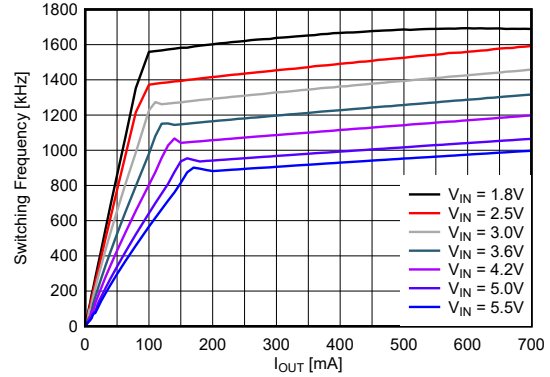


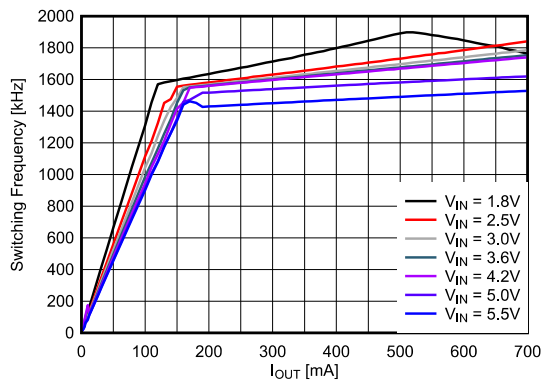
Figure 9-7. Output Voltage vs Output Current at 1.2 V<sub>OUT</sub>



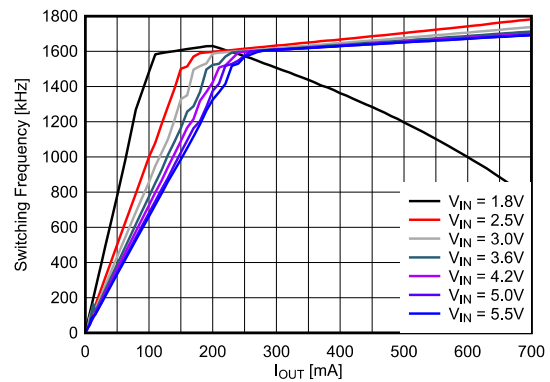
**Figure 9-8. Output Voltage vs Output Current at 0.7  $V_{OUT}$**



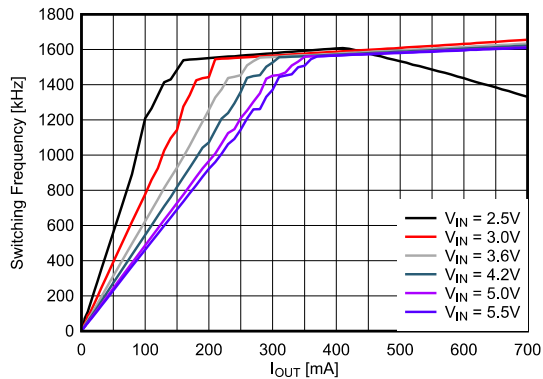
**Figure 9-9. Switching Frequency vs Output Current at 0.4  $V_{OUT}$**



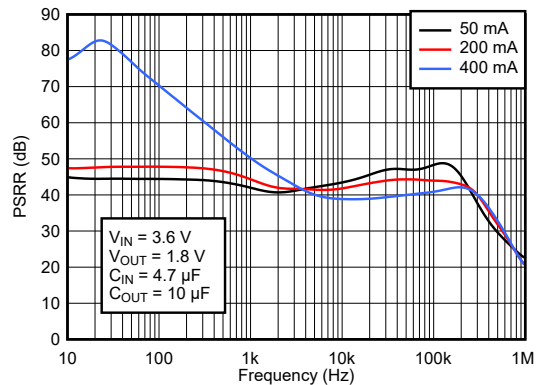
**Figure 9-10. Switching Frequency vs Output Current at 0.7  $V_{OUT}$**



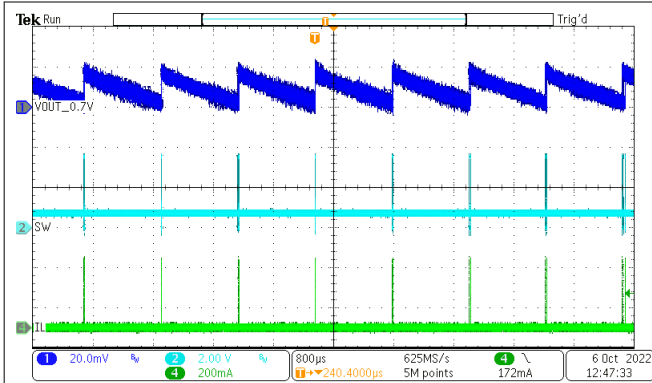
**Figure 9-11. Switching Frequency vs Output Current at 1.2  $V_{OUT}$**



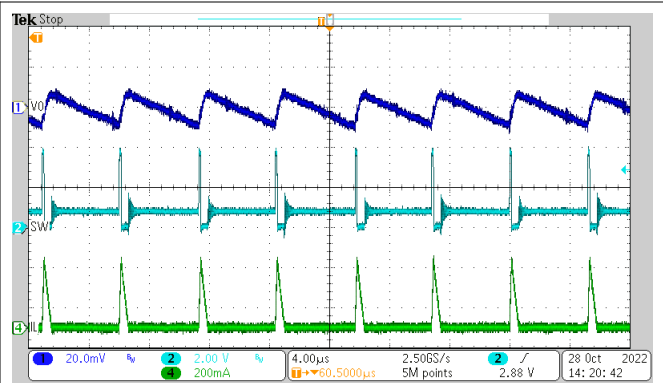
**Figure 9-12. Switching Frequency vs Output Current at 1.8  $V_{OUT}$**



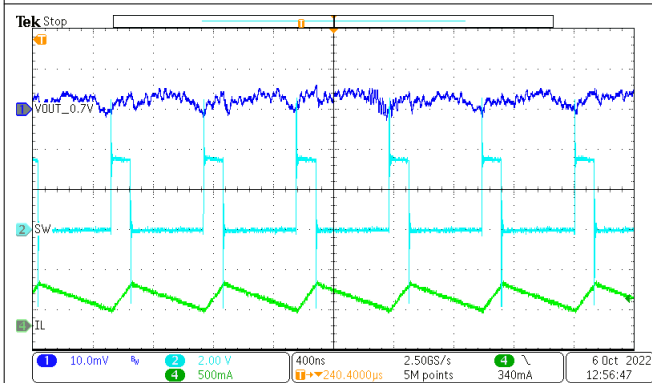
**Figure 9-13. Power Supply Rejection Ratio (PSRR) at 1.8  $V_{OUT}$**



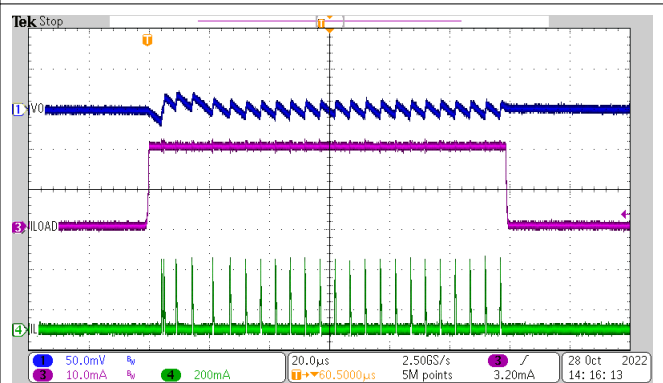
**Figure 9-14. Typical Operation at 0.7 V<sub>OUT</sub>, 100 μA I<sub>OUT</sub>**



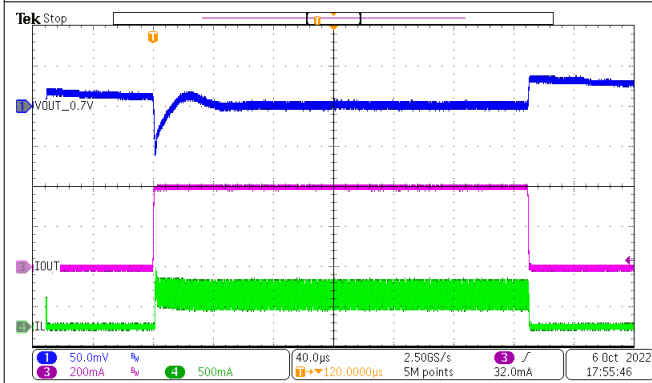
**Figure 9-15. Typical Operation at 0.7 V<sub>OUT</sub>, 20 mA I<sub>OUT</sub>**



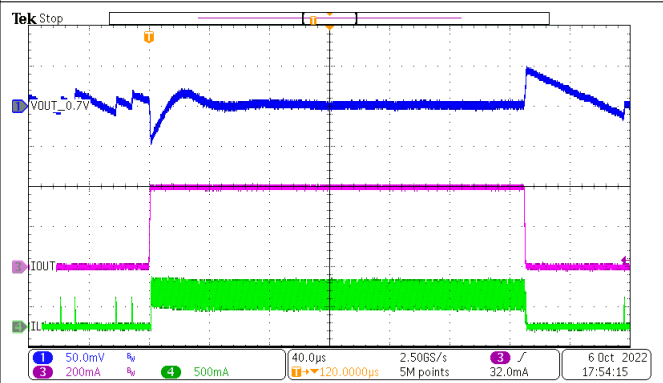
**Figure 9-16. Typical Operation at 0.7 V<sub>OUT</sub>, 400 mA I<sub>OUT</sub>**



**Figure 9-17. Load Transient at 0.7 V<sub>OUT</sub>, I<sub>OUT</sub> = 100 μA to 20 mA**

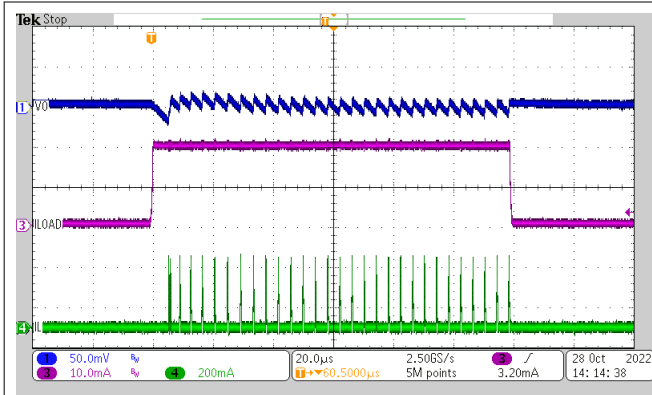


**Figure 9-18. Load Transient at 0.7 V<sub>OUT</sub>, I<sub>OUT</sub> = 100 μA to 400 mA**

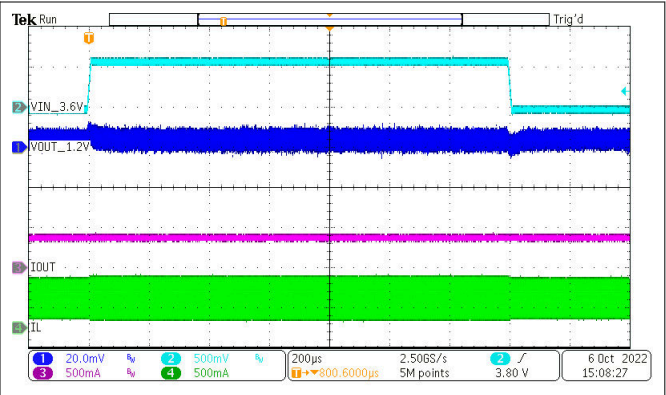


**Figure 9-19. Load Transient at 0.7 V<sub>OUT</sub>, I<sub>OUT</sub> = 5 mA to 400 mA**

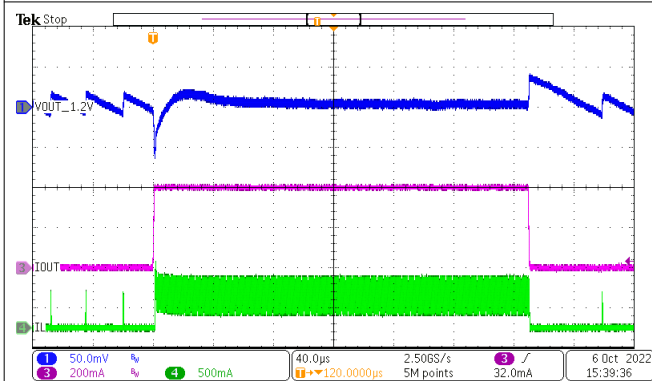




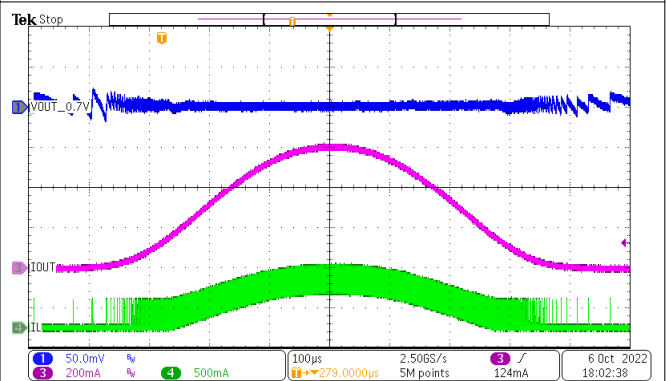
**Figure 9-20. Load Transient at 1.2 V<sub>OUT</sub>, I<sub>OUT</sub> = 100 µA to 20 mA**



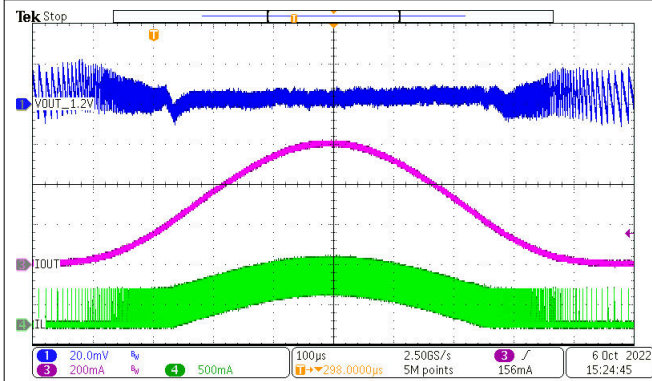
**Figure 9-21. Load Transient at 1.2 V<sub>OUT</sub>, I<sub>OUT</sub> = 100 µA to 400 mA**



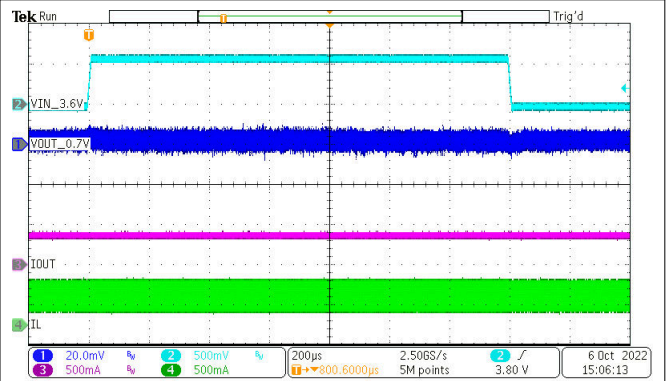
**Figure 9-22. Load Transient at 1.2 V<sub>OUT</sub>, I<sub>OUT</sub> = 5 mA to 400 mA**



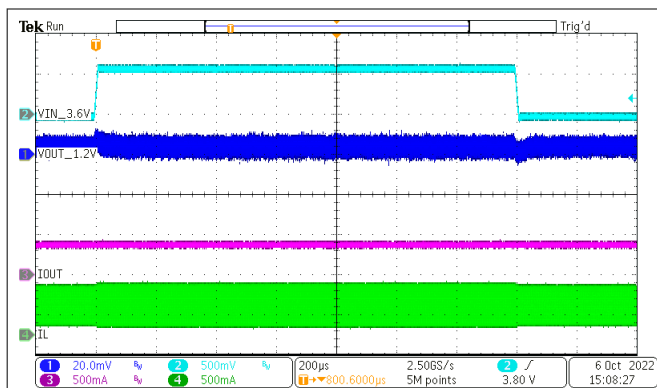
**Figure 9-23. AC Load Sweep at 0.7 V<sub>OUT</sub>, I<sub>OUT</sub> = 1 mA to 600 mA**



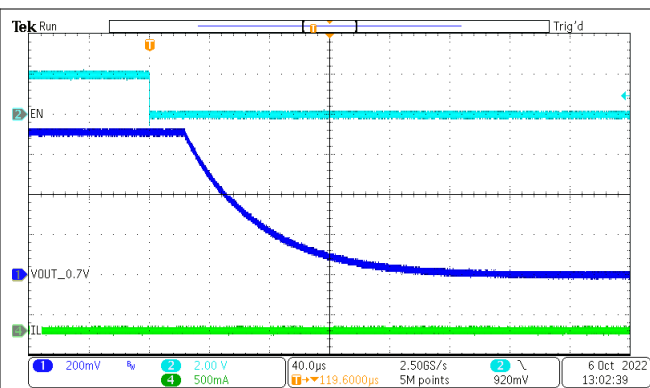
**Figure 9-24. AC Load Sweep at 1.2 V<sub>OUT</sub>, I<sub>OUT</sub> = 1 mA to 600 mA**



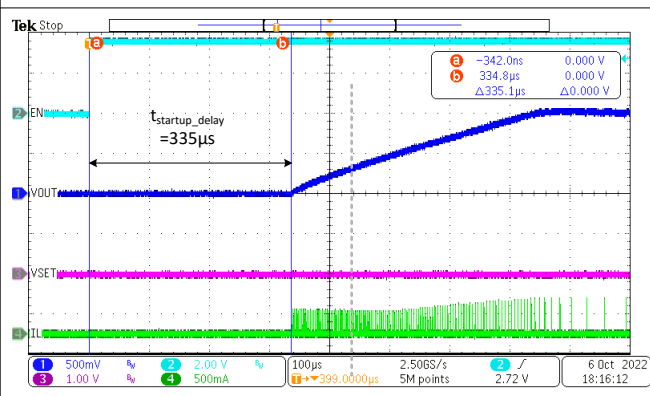
**Figure 9-25. Line Transient at 0.7 V<sub>OUT</sub>, I<sub>OUT</sub> = 400 mA, V<sub>IN</sub> = 3.6 V to 4.2 V**



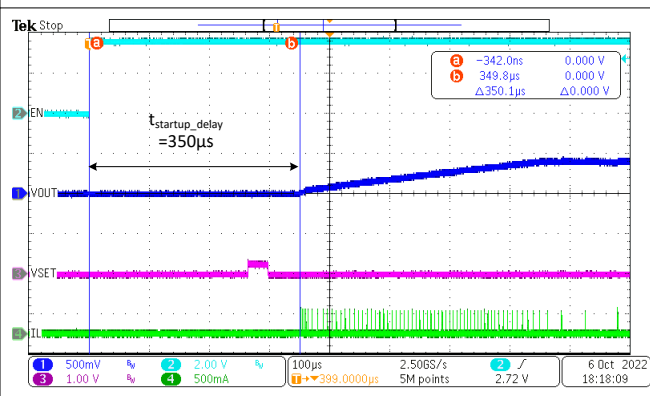
**Figure 9-26. Line Transient at 1.2 V<sub>OUT</sub>, I<sub>OUT</sub> = 400 mA, V<sub>IN</sub> = 3.6 V to 4.2 V**



**Figure 9-27. Shutdown, Output Discharge at 0.7 V<sub>OUT</sub>**



**Figure 9-28. Start-Up Delay Time, VSET = GND**



**Figure 9-29. Start-Up Delay Time, VSET = 10 kohms**

## 9.3 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage, and output current of the TPS62843.

## 9.4 Layout

### 9.4.1 Layout Guidelines

The pinout of TPS62843 has been optimized to enable a single top layer PCB routing of the IC and its critical passive components such as C<sub>IN</sub>, C<sub>OUT</sub>, and L. Furthermore, this pinout allows the user to connect tiny components such as 0201 (0603) size capacitors and 0402 (1005) size inductors. A solution size smaller than 5 mm<sup>2</sup> can be achieved with a fixed output voltage. As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance. Providing a low inductance, low impedance ground path is critical. Therefore, use wide and short traces for the main current paths. Place the input capacitor as close as possible to the V<sub>IN</sub> of the IC and GND pins. This placement is the most critical component placement. The V<sub>OS</sub> line is a sensitive, high impedance line and must be connected to the output capacitor and routed away from noisy components and traces (for example, the SW line) or other noise sources.

### 9.4.2 Layout Example

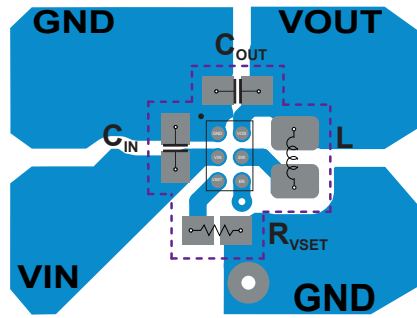


Figure 9-30. Layout Example (YKA Package)

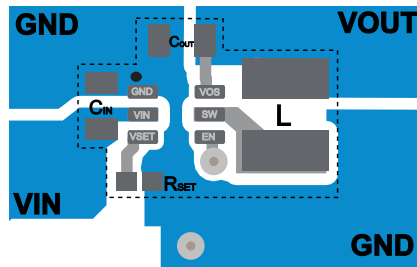


Figure 9-31. Layout Example (DRL Package)

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Device Support

#### 10.1.1 Third-Party Products Disclaimer

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#### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 10.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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#### 10.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 10.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS628436YKAR    | ACTIVE        | DSBGA        | YKA             | 6    | 12000       | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 125   | J                       | <a href="#">Samples</a> |
| TPS628437YKAR    | ACTIVE        | DSBGA        | YKA             | 6    | 12000       | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 125   | K                       | <a href="#">Samples</a> |
| TPS628438YKAR    | ACTIVE        | DSBGA        | YKA             | 6    | 12000       | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 125   | L                       | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ   | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|-------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS628436YKAR | DSBGA        | YKA             | 6    | 12000 | 180.0              | 8.4                | 0.9     | 1.16    | 0.47    | 2.0     | 8.0    | Q1            |
| TPS628437YKAR | DSBGA        | YKA             | 6    | 12000 | 180.0              | 8.4                | 0.9     | 1.16    | 0.47    | 2.0     | 8.0    | Q1            |
| TPS628438YKAR | DSBGA        | YKA             | 6    | 12000 | 180.0              | 8.4                | 0.9     | 1.16    | 0.47    | 2.0     | 8.0    | Q1            |

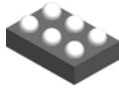


**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ   | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|-------|-------------|------------|-------------|
| TPS628436YKAR | DSBGA        | YKA             | 6    | 12000 | 182.0       | 182.0      | 20.0        |
| TPS628437YKAR | DSBGA        | YKA             | 6    | 12000 | 182.0       | 182.0      | 20.0        |
| TPS628438YKAR | DSBGA        | YKA             | 6    | 12000 | 182.0       | 182.0      | 20.0        |

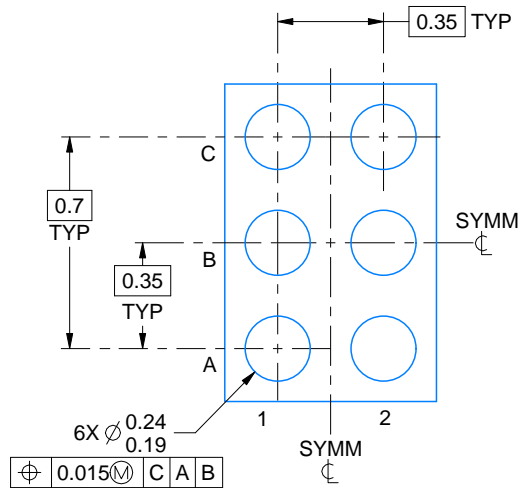
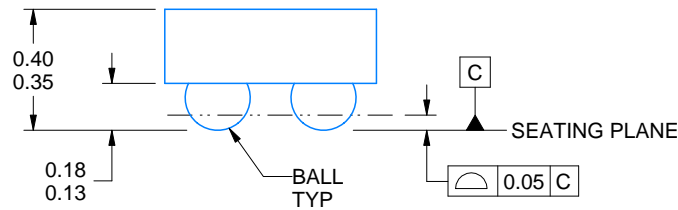
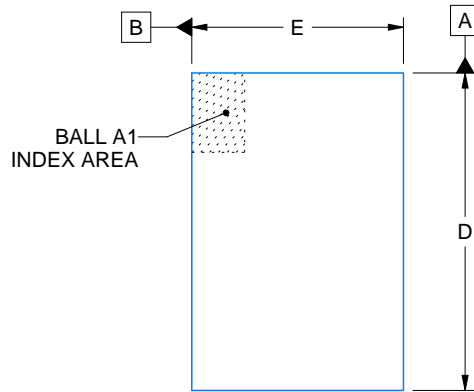
YKA0006



PACKAGE OUTLINE

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.04 mm, Min = 0.98 mm  
E: Max = 0.787 mm, Min = 0.727 mm

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NOTES:

NanoFree is a trademark of Texas Instruments.

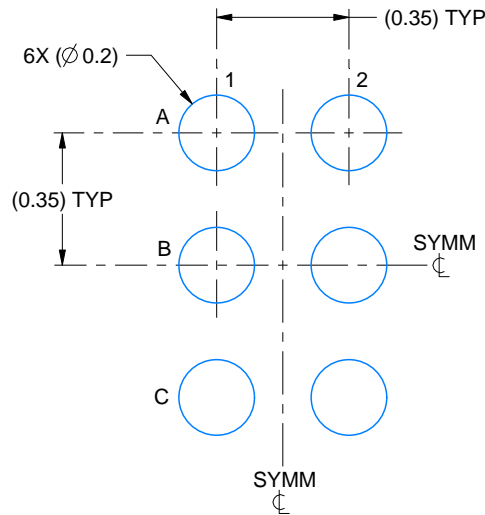
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

# EXAMPLE BOARD LAYOUT

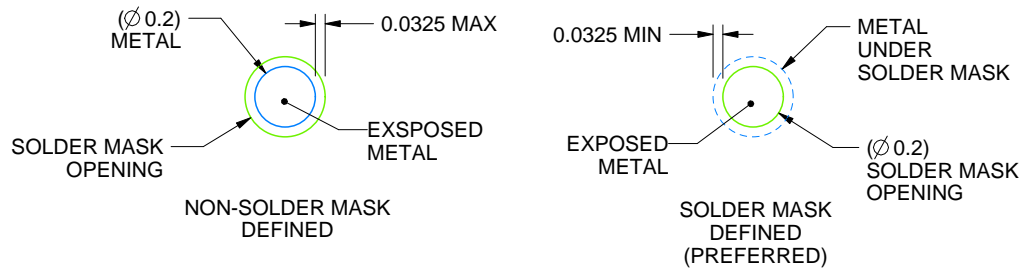
YKA0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:50X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

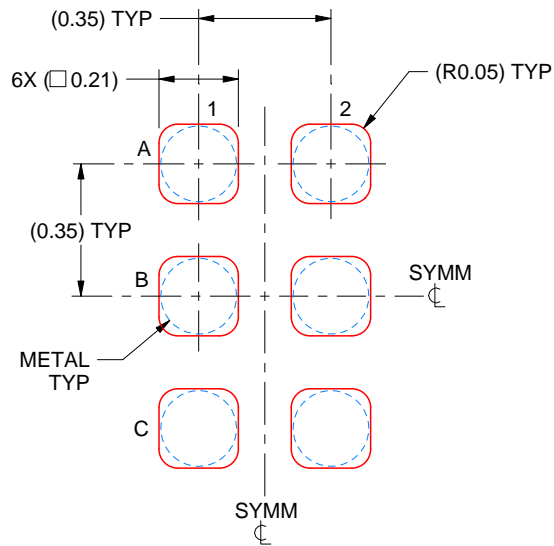
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YKA0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.075 mm - 0.1 mm THICK STENCIL  
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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